IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : **M. Takada, H. Minoura, H. Kobayashi K. Tsukada, and M. Kondo**

Examiner: **R. Beddering**

#10 Ext. of Time (1) Amdt C 1/11/02 R. Tyson

Application No.: **09/380,994**

Group Art Unit: **2841**

Filing Date: **September 13, 1999**

S&L Docket No.: **23,128**

For: **PRINTED WIRING BOARD AND METHOD FOR MANUFACTURING SAME**

CERTIFICATE OF MAILING

I hereby certify that this correspondence, along with any papers indicated as being enclosed, are being deposited as First Class Mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on October 30, 2001.

10-30-01
Date

Denise Grisack
Denise Grisack

The Commissioner for Patents
Washington, DC 20231

RESPONSE TO FIRST OFFICE ACTION

Sir:

In view of the following amendments and remarks responsive to the first Office Action of July 5, 2001, Applicant respectfully requests favorable reconsideration of this application.

In the Drawings

Applicant submits herewith copies of the drawings showing proposed drawing changes marked in red. The proposed changes are submitted in response to objections to the drawings set forth in the Office Action and are discussed below in the REMARKS section. Applicant respectfully requests the Office to approve the proposed drawing changes and, subject to such approval, will submit corrected formal drawings in accordance therewith after receipt of a Notice of Allowability in this case.

In the Claims

Please amend the claims as noted below:

1. (Once Amended) A printed wiring board comprising an odd number n of conductive layers which are built up with an odd number of insulating layers respectively and are electrically connected to one another by interconnecting through holes;

wherein the first conductive later is a component-connecting layer on which an electronic component is to be mounted and conducts electric currents in and out of the electronic component; the n-th conductive layer is an external connecting layer for connecting external connecting terminals which conducts electric currents in and out of the printed wiring board; the second to (n-1)-th conductive layers are current transmitting layers for transmitting internal currents of the printed wiring board; and the

surface fo the n-th conductive layer is covered with the n-th and outermost insulating layer with external connecting terminals being exposed, and wherein a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring.

3. (Twice Amended) A method of manufacturing a printed wiring board having an odd number n of conductive layers which are built up with an odd number of insulating layers respectively and are electrically connected to one another by interconnecting through holes, the method comprising the steps of:

interposing insulating layers between the second to n-th conductive layers respectively and also forming first interconnecting through holes for electrically connecting the conductive layers to one another;

laminating a first prepreg and a copper foil on a surface of the second conductive layer, and press-bonding a second prepreg on a surface of the n-th conductive layer to form a multilayer substrate having an odd number n of insulating layers, wherein the second to n-th conductive layers are internal layers of the multilayer substrate;

etching the copper foil to form a first conductive layer;

forming second interconnecting through holes in the first insulating layer and forming connecting holes in the n-th insulating layer respectively;

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forming a metal plating film for electrically connecting the first conductive layer with the second conductive layer on the walls of the second interconnecting through holes of the first insulating layer; and

connecting external connecting terminals to the surface of the n-th conductive layer exposed through the connecting holes of the n-th insulating layer.

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4. (Twice Amended) A printed wiring board comprising an internal insulating substrate having a conductor circuit formed on a surface thereof, an internal insulating layer laminated on the surface of the internal insulating substrate, and an external insulating layer laminated on a surface of the internal insulating layer, the internal insulating layer and the external insulating layer having an internal conductor circuit and an external conductor circuit respectively;

wherein the internal insulating layer comprises two or more internal insulating layers of glass cloth-reinforced prepreg.

In the Abstract

Please amend the abstract as noted on the attached sheet.

REMARKS

Applicant respectfully thanks the Office for the indication that claims 15 and 18 are allowed.

A. Non-Art Rejections and Objections

In Section 1 of the Office Action, Office vacated the previous restriction requirement. Accordingly, all original claims were examined except for claims that Applicant cancelled in it's response to the restriction requirement. Particularly, as the Office has correctly noted, those claim cancellations were made by Applicant for reasons unrelated to the restriction requirement.

In Section 2 of the Office Action, the Office noted that the supplemental page of the Declaration which contains the numbers of the last two priority documents is missing from the application. Applicant's attorney's records indicate that the supplemental page of the Declaration was submitted with the application. Presumably, it was misplaced in the Office. In any event, enclosed herewith is a copy of the supplemental page of the Declaration, which should make the Office's records complete in this regard.

In Section 4 of the Office Action, the Office objected to the drawings for having improper crosshatching and referred to page 600-84 and §608.2 of the M.P.E.P. and required drawing corrections. The Office further stated that the drawing correction submitted September 13, 1999 are not approve because they do not correct the crosshatching problem and that Applicant must include the changes submitted September 13,1999 in any new set of drawing corrections submitted herewith. Accordingly, Applicant submits herewith proposed drawing corrections with the corrections marked in red. The attached drawings correct the crosshatching matter and

further reflect the same changes offered in the proposed drawing corrections submitted on September 13, 1999.

Applicant respectfully requests the Office's approval of these proposed drawing changes.

In Section 5 of the Office Action, the Office objected to the Abstract stating that the words "constitute" and "constituted" are not understood in the context. While Applicant disagrees with the Office and believes that those terms are sufficiently clear as used in the Abstract, Applicant has nonetheless amended the abstract in order to eliminate the use of those words. Applicant also has corrected one other grammatical error.

In Section 6 of the Office Action, the Office requested Applicant to replace the word "via" with the word "with" or "by" and to replace the word "leads" with the word "conducts" in all of the claims. Particularly, the Office asserted that the words "via" and "leads" are terms of art referring to through holes and terminals and, therefore, their usage in the claims is confusing. The Office's position is well taken. Applicant has herein amended the claims accordingly.

B. Art Rejections

In Section 8 of the Office Action, the Office also rejected (a) claims 1, 2, and 4 under the 35 U.S.C. §102(e) as anticipated by Figure 1 of Feilchenfeld, (b) claims 11 and 14 under 35 U.S.C. §102(b) as anticipated by cavity 118 of Figure 10 of Brown, and (c) claims 3, 7, and 10 under 35 U.S.C. §103(a) as unpatentable over Feilchenfeld.

Actually, the rejection of claims 11 and 14 in the Office Action did not identify the prior art reference on which the Office was relying. However, since the rejection mentions cavity 118 and openings 176, 178 of Figure 10 of the reference, Applicant presumes that the reference of interest is Brown (US Patent No, 4,729,061). That is the only prior art reference of record that appears to have a Figure 10 with a cavity 118 and openings 176, 178.

As previously noted, claims 15 and 18 are allowed.

1. Claims 1 and 2

The present invention as recited in claim 1 relates to a built up printed wiring board (PWB) having an odd number n of conductive layers such that the middle layer, i.e., layer number (n+1)/2, is in the center of the stack and has the same number of insulating layers above it and below it. This prevents warping of the PWB during press bonding of prepregs for forming the insulating layers. Claim 1 clearly recites the above-mentioned features. Particularly, claim 1 recites "a printed wiring board comprising an odd number n of conductive layers which are built up with an odd number of insulating layers". The claim, as amended herein now even further recites "and wherein a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring board".

Feilchenfeld, on the other hand, teaches none of a built up type wiring board, an odd number of insulating layers, or a central insulating layer that prevents warping.

Specifically, Feilchenfeld is directed to an organic chip carrier 10 with conductive layers 12, 18, 20, 25, 32, and insulating layers 14, 16, 22 and 24 that are alternately

arranged. Feilchenfeld's chip carrier is not a built up type PWB. Further, Feilchenfeld discloses an even number of insulating layers (14, 16, 22, and 24). Accordingly, it also does not disclose a central insulating layer that prevents warping. Accordingly, Feilchenfeld essentially discloses a conventional chip carrier that contains none of the features that Applicant considers to be its invention.

Accordingly, claim 1 distinguishes over Feilchenfeld baed on the distinctions discussed above.

Claim 2 depends from claim 1 and therefore distinguishes over Feilchenfeld on the same basis.

2. Claim 4

With respect to claim 4, applicant has amended this claim to recite that the "internal insulating layer is of a glass cloth-reinforced prepreg", a limitation that existed in claim 4 as originally filed, but which was removed by preliminary amendment. As discussed on page 40, lines 7-18 of the present specification, the use of a glass cloth-reinforced prepreg for internal layers lowers the coefficient of water absorption and enhances the adhesion between the layers for the internal layers s. Feilchenfeld does not teach or suggest employing a glass cloth-reinforced prepreg for the internal layers. Rather Feilchenfeld discloses only that the first and second inner layers 14, 16 are formed of polytetraflourethylene (PTFE) (see col. 4, lines 55-60).

Accordingly, claim 4 distinguishes over Feilchenfeld.

3. Claims 11 and 14

With respect to the prior art rejection of claims 11 and 14 in view of Brown, Applicant respectfully traverses. Claims 11 and 14 are directed to a PWB having a covering pad covering one opening of an interconnecting through hole and a conductor circuit provided along the peripheral edge of the other opening with a solder ball bonded on to the surface of the covering pad.

With this design, real estate on the PWB is conserved because the solder ball can be located very close to the through hole. See page 19, lines 18-28 of the specification.

Brown, on the other hand, is directed to a PCB having cavities 118 for mounting a circuit die therein. It also shows a multilayer PCB with through holes 160. However, those through holes are neither covered nor have a solder ball thereon. In fact, the statement in the Office Action that claims 11 and 14 are "clearly anticipated by cavities (118) of Figure 10" suggest that the Office has misunderstood the reference. Cavity 118 is not a through hole. Rather, it is a cavity in only the top layer of the PCB in which the die 154 is mounted. The die is then covered with encapsulant 158. Accordingly, cavity 118 has nothing to do with through holes and the subject matter of the present invention. Clearly cavity 118 is not "an interconnecting through hole penetrating an insulating substrate" as recited in claim 11, nor does it have "a conductor circuit provided along the peripheral edge of the other opening" of the through hole. There is no other opening of cavity 118 in Brown because it does not pass completely through the PWB. Even further, even if encapsulant 158 is somehow considered to meet the "covering pad" limitation, there is no rational way to view Brown as meeting the

limitation that "the covering pad and the conductor circuit are electrically connected to each other via a metal plating film covering a wall of the interconnecting through hole".

Even further, certainly there is no solder ball disclosed in Brown, either related to cavity 118 or the actual through holes, e.g., 160. The through holes disclosed in Brown are standard through holes without covering pads or solder.

In essence, beyond disclosing a printed circuit board with through holes (which Applicant does not dispute is known in the prior art), the Brown reference is irrelevant.

Accordingly, claim 11 distinguishes over Brown.

Claim 14 depends from claim 11 and therefore distinguishes over the prior art for the same reasons discussed above in connection with claim 11.

4. Claims 3, 7 and 10

Finally, the Office rejected claims 3, 7 and 10 as obvious over Feilchenfeld.

Applicant respectfully traverses this rejection. Addressing claim 3 first, this claim is an independent method claim counterpart to independent apparatus claim 1 and contains the same pertinent limitations. For instance, claim 3 recites "a printed wiring board having an odd number and of conductive layers which are built up with an odd number of insulating layers". Accordingly, claim 3 distinguishes over the prior art for all of the same reasons discussed above in connection with claim 1.

With respect to claim 7, it recites a method of manufacturing a PWB with a plurality of built up conductive and insulating layers with connecting through holes and including the steps of "covering the walls of the interconnecting through holes with metal plating films" and "fusing solder balls against the interconnecting through holes

and filling them with solder". As discussed on page 16, lines 10-17 of the specification, the metal plating on the walls of the through holes helps with the conductivity of the through holes. Further, the solder and solder balls enable electric currents to flow across the internal conductive layers so that the signals can be taken out easily through the solder and solder balls. Applicant has reviewed Feilchenfeld and has found no disclosure of either covering the walls of the interconnecting through holes with metal plating films or solder or of using solder balls at the openings of the interconnecting through holes. Accordingly, Feilchenfeld does not contain any disclosure relevant to the above-quoted features of claim 7.

Claim 10 depends from claim 7 and therefore distinguishes over the prior art of record for all the same reasons discussed in connection with claim 7. Accordingly, the rejection of claim 7 should be withdrawn.

C. Conclusion

In view of the foregoing comments, all of the pending claims have been shown to be allowable over the prior art of record. Applicant also has herein addressed all other matters raised in the Office Action. Accordingly, in view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

In the Abstract

Please amend the Abstract as noted on the attached sheet.

In a printed wiring board, an odd number (n) of conductive layers (11-13) and insulating layers (21-23) are alternately laminated upon each other. The first conductive layer (11) is a parts connecting layer and the n-th conductive layer (13) is an external connecting layer which is connected to external connecting terminals (7). The second to (n-1)-th conductive layers (12) are current transmitting layers for transmitting internal currents. The surface of the n-th insulating layer (23) in a state where the external connecting terminals (7) are exposed on the surface. It is preferable to make the initial insulating layers of a glass-cloth reinforced prepreg and the external insulating layers of a resin.

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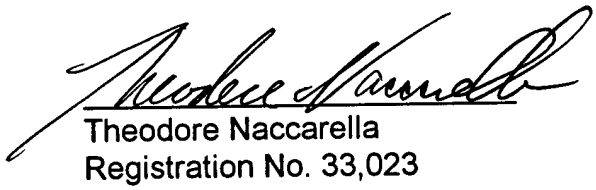
Respectfully submitted,



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